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IMPLEMENTING THE TETRA PHYSICAL LAYER ON LYRTECH'S SFF SDR DEVELOPMENT PLATFORM

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Abstract¹ section: 4.2 Waveform design, performance evaluation, development process, validation process

EXTENDED ABSTRACT

This paper presents the implementation of the TETRA physical layer on an FPGA/DSP based development platform. The objective is to implement a highly portable waveform and to evaluate where to set the boundary between FPGA-functions and DSP-functions. Due to the portability aspect, we tried to implement as much functionality as possible on the DSP and followed a design process proposed from the Model Driven Architecture. The Lyrtech Small Form Factor SDR Development Platform is used as the hardware platform. It is equipped with a Virtex-4 SX35 FPGA from Xilinx and a TMS320DM6446 DSP system-on-chip from Texas Instruments.

a) TETRA System Overview

Terrestrial Trunked Radio (TETRA) is an open digital standard defined by the European Telecommunication Standards Institute (ETSI). Its infrastructure is primarily targeted at the mobile radio needs of public safety groups like police and fire departments.

For modulation a $\pi/4$ -Differential Quaternary Phase Shift Keying (DQPSK) scheme is used which provides a baud rate of 18 kbaud/s. TETRA uses different forward error correction schemes applied to the different logical channels. For the Traffic Channel (TCH) a Rate Compatible Punctured Code (RCPC) is employed while the Access Assignment Channel (AACH) uses a shortened Reed Muller (RM) code for example. The channel access mode is a combination of FDMA and TDMA. Each carrier providing a bandwidth of 25 kHz is divided into 4 timeslots. For

Uplink/Downlink separation an FDD/TDD mode is implemented. The time delay on the uplink is about two time slots against the downlink, so the mobile station does not have to send and receive data simultaneously. Within one time slot of each carrier frequency a normal burst is transmitted. It is used for the transmission of voice or data and contains 432 data bits and 78 bits for training, synchronization, guard period, etc. So the overall length of a burst is 510 bits that are transmitted within 14.17 ms. Four bursts fit into one TDMA frame which results in a frame duration of 56.67 ms.

b) Waveform Development

One objective of this work was to get a high portability of the TETRA-waveform and to evaluate if modules could be reused. We followed a waveform based development process based on the Model Driven Architecture (MDA) which is an initiative of the Object Management Group (OMG). The MDA introduces different types of models:

1. The Computation Independent Model
2. The Platform Independent Model
3. The Platform Specific Model
4. The Code

These models are levels of abstraction of a waveform. By implementing all these models there is an evolution from a very generic waveform specification to code which can be executed on hardware.

The Computation Independent Model (CIM) is just a description of the functionality. In our case, this is the specification of the TETRA air interface, i.e. the ETSI standard. The next model is a Platform Independent Model (PIM) that provides the functionality without platform specific aspects. The PIM was created by implementing a MatLab/Simulink model of the TETRA physical layer. There are seven different bursts defined in the specification. For simplicity we decided to implement just the Normal Continuous Downlink Burst. This burst includes a Traffic Channel for the data supporting a bit rate of 4.8 kbit/s (TCH/4.8) and a Control Channel (CCH) that manages the allocation of the next up- and downlink slots.

¹ The authors agree that the paper may be reviewed by the SDR Forum paper evaluation committee for purposes of inclusion in the conference. The authors allow the inclusion of the paper in SDR Forum conference publications, and other SDR Forum publications, if the paper is accepted.

The next step suggested from the MDA is the design of a Platform Specific Model (PSM) that includes platform specific aspects. To transform the PIM to the PSM we followed the design flow proposed by Lyrtech. Due to that, we replaced the generic blocks in the model by target specific blocks. We additionally added platform specific blocks that are interfacing the I/Os on the board.

To create a PSM there was the need to decide which functions run on the FPGA and which on the DSP. The higher the flexibility of a processor, the higher its code reusability. But unfortunately the result is a decrease of performance. Due to this we evaluated how much functionality we could bring into the DSP without using the FPGA and how much the DSP is disburdened if we take functions back to the FPGA.

The final step in the MDA is the implementation of Code that runs on the specific platform. The development environment generates code from the PSM and sends it to the processors Integrated Development Environment (IDE), that will compile the generated code and load the executables to the processors.

We are going to present the implementation of the TETRA physical layer on Lyrtech's SFF SDR development platform. We further present a design flow that combines the waveform development of the MDA with the design flow proposed by Lyrtech. Additionally we will evaluate the partition of the PSM in an FPGA part and a DSP part and further we will consider which functions are useful to run on the DSP or on the FPGA.

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