Wideband Receiver for a Spaceborne Software Radio Application

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Abstract- **Software Defined Radio (SDR), thanks to the recent technological advancements, has become one of the valuable solutions to achieve flexibility in a regenerative communication payload on board the satellite. However, in order to take advantage of all its potentialities much work needs still to be done to overcome the related bottlenecks. This paper reports part of the feasibility study on an advanced receiver front end design capable of digitizing more than 300 MHz bandwidth. In particular, it describes the reasons behind the selected front-end architecture and provides the conclusions of a preliminary system analysis for the receiver linearity. Finally, a list of candidate baseband processing algorithms for the compensation of one of the receiver RF impairments is presented.**

Index Terms- **Digital front-end, wideband receiver, IIP3, ADC requirements, RF front-end, software-defined radio, I/Q imbalance compensation, cross modulation.**

I. INTRODUCTION

Software Defined Radio (SDR) represents a precious alternative solution for the satellite on-board processing flexibility necessary to achieve the communication payload agility required by many satellite operators.

The key advantage is the outstanding improvement of the payload functionalities in terms of upgrading capabilities for the communication standards, adaptive modifications of the payload mission and development of new access schemes for the satellite services (i.e. adaptive modulation and coding) [1].

In this paper, part of the preliminary feasibility study for an SDR application on-board the satellite is presented. The referred application is the LuxSpace proposal for the next generation payload of the Orbcomm satellite constellation, it is called ALOA (Advanced Low-earth Orbit Communication).

The Orbcomm system is a commercial, satellite-based, wireless telecommunications network designed to send and receive data from anywhere in the world. The network provides global data communications, narrowband two-way digital messaging and geo-positioning services through a constellation, currently consisting of 30 Low-Earth Orbit (LEO) satellites, and terrestrial gateways located around the world.

ALOA will provide a set of Core Services, namely the Orbcomm VHF Messaging Service and the AIS (Automatic Identification System) for ships, but will also be able to support new RF based Services for civil, military and/or dual use applications [2].

Flexibility is considered as a must for ALOA on-board processing (OBP), as it will provide the possibility to modify the payload features/performances, during assembly, integration and test (AIT) and/or in-flight, during its full lifetime, thanks to physical insertions/replacements and/or through new software integration/uploads [2].

Hereafter, the attention is focused on its receiver architecture, in particular to its front-end part that represents one of the main bottlenecks for any SDR implementation [3].

The paper is divided in two main sections: the first discusses the selected front-end architecture for the cited application and lists some results of the preliminary receiver linearity analysis; the second reports some considerations on candidate digital compensation methods for the I/Q imbalance.

As preliminary approach, it has not been considered the usage of space-qualified components, as the main target of this study phase has been the identification of possible showstoppers for the design concept.

Finally, conclusions are drawn in the last section.

II. RECEIVER FRONT-END

As previously cited, ALOA payload has to undertake different services, like messaging and geo-positioning, whose channels are allocated in a ~ 300 MHz bandwidth in the VHF and UHF frequency bands. Every set of channels occupies a different bandwidth, thus enhancing filtering complexity.

In addition, since software re-configurability is easily accomplished by shifting as much of the analog signal-processing tasks as possible into the digital domain [9], the candidate front-end should then allow digital access to the entire system bandwidth, still satisfying the selectivity imposed by the application requirements.

A "digital IF" solution, where the signal is first converted to an intermediate frequency (IF) and then digitized, with a second mixing stage in the digital domain, is here unrealistic because of the extremely demanding specifications on the ADC component (1 Gsps and more than 14 bits of resolution). Also, given the low frequency band of the application, a super-heterodyne architecture would add redundant components, making the receiver too bulky and power-hungry [6][7].

Based on the considerations above, the analysis has thus been focused on a direct-conversion architecture, detailed in FIGURE 1. In such architecture the RF signal is converted directly to baseband, thus reducing the necessary number of analog components. Besides, it represents a suitable solution for a frequency band flexible solution, as most of its functionalities can be carried out by the digital section.

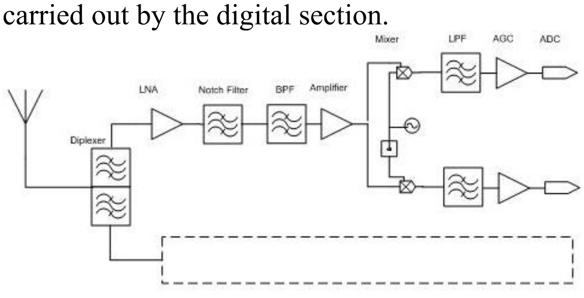

FIGURE 1: ALOA receiver architecture

The receiver architecture shown in FIGURE 1 presents four filtering stages (diplexer, notch filter, band-pass filter and anti-aliasing low pass filter), three amplifiers (one of which performing AGC functionalities), mixing and data conversion stages.

A. ADC selection and overall gain value

One possible showstopper, given the bandwidth to be digitized (totally 312 MHz), is the ADC (Analog-to Digital Converter), whose requirements for an SDR application can be very demanding in terms of required dynamic range and linearity.

In TABLE 1 the specifications of one of the ALOA services are reported.

Parameters	Specifications
Uplink band B	3840 Hz
Receiver sensitivity	-110 dBm
CNR[1]	23 dB
Maximum tone power	-76 dBm
Max noise figure	3 dB[2]

TABLE 1: ALOA receiver specification

The suitable ADC has to provide the minimum sampling rate for the system bandwidth. For a commercial ADC (ADS5474 from Texas Instruments [4]) with 500 MHz sampling rate and 14 bit of resolution, this task is nowadays easily achieved. Indeed, applying a sampling factor equal to 2.2 to the baseband bandwidth it results that the ADC has to provide a sampling rate of about 350 Msps, far away from its maximal performances.

As second step, the minimum value for the gain of the components cascade has been identified. The overall gain of the components between the antenna and the ADC has indeed been computed by analyzing the minimum detectable signal (MDS) after the conversion stage [5].

The MDS is defined to be equal to the total noise power within the 322 MHz noise equivalent bandwidth of the receiver (derived from the band-pass filter before the mixer stage). In general, it is given by:

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[1] $$CNR = \frac{E_b}{N_o} + 10 \times \log_{10}(R_b / B)$$

with Rb and B equal respectively to the data rate and uplink band of the referred service.

[2] This noise figure value obeys also to other constraints derived from the overall link budget analysis.

$$MDS = 10 \times \log_{10}(K \times T \times BW) + NF \qquad (1)$$

where K is the Boltzman´s costant (1.38×10^{-23} Ws/K), BW is the systems bandwidth, T is the absolute temperature at the input of the receiver and NF is the total noise figure. Using the values in TABLE 1:

$$MDS = -85.92[dBm] \qquad (2)$$

Typically, in order to retrieve the total gain of the components cascade before the ADC, it is enough to consider that the noise power at the input to the ADC has to be higher than its noise power [5].
Therefore, considering that the selected ADC has 2.5 W of power dissipation, full scale voltage of 2.2 V and an input impedance of 500 Ω, the full scale power is thus 0.83 dBm. Moreover, since the dynamic range of this device is:

$$DR(dB) = ENOB \times 6.02 + 1.76 = 67.38[dB] \qquad (3)$$

with ENOB equal to 10.9 [bit] [4], it follows that the ADC noise power is about -68.9 dBm.
Finally, if we consider then that the noise power at the input of the ADC is

$$N_{ADC\_in} = MDS + G \qquad (4)$$

where G is the gain between the antenna and the ADC , according to [5],

$$G > -68.9 - MDS \qquad (5)$$

that in our case it translates in G > 20 dB.
In conclusion, the preliminary ADC selection imposes an overall gain of at least 20 dB to be distributed among the shown components.

A. Receiver linearity analysis

With regard to the linearity of the receiver, both second order and third order distortion need to be considered. Indeed, as in the direct-conversion receiver the signal is converted directly to base-band, the second order linearity of the mixer has direct influence on the desired signal dynamic range [7].
Furthermore, as the third order distortion of the LNA is responsible for the single tone desensitization and cross modulation events [7], special attention has to be paid in the selection of this component.
In TABLE 2 the assumed interference environment is presented: the table reports the single tone and the two blocking tones interference power level.

Parameters	Assumed values
Single tone power	-60 dBm
Two tone power	-62 dBm

TABLE 2: Interference environment

From the two tones interference it is possible to retrieve the requirement for the receiver input referred third order intercept point (IIP3).
By applying,

$$IIP3_{total}[dBm] = 1/2 \times (3 \times I - N) \qquad (6)$$

where I is the two tone power in TABLE 2 and N is the noise power in the channel band (3840 Hz); it ensues that the receiver IIP3 has to be no less than -25.42 dBm.
In addition, the overall 1dB compression point of the receiver has to be high enough in order not to saturate the highest signal in input.
Based on these considerations, TABLE 3 shows the complete list of linearity requirements for the proposed application.

Parameters	Retrieved values
IIP3 receiver	-25.42 dBm
P1db @ input	-75 dBm
IIP2 mixer	55 dBm
IIP3 LNA	26.55 dBm

TABLE 3: receiver linearity requirements.

In order to carry out the trade-offs between linearity and noise figure of the component, the following formulas (in linear) have been used [7]:

$$\frac{1}{IIP3^2_{total}} = \frac{1}{IIP3_1^2} + \sum_{i=2}^{n} \frac{G_1^2 G_2^2 ... G_{i-1}^2}{IIP3_i^2} \qquad (7)$$

$$\frac{1}{IIP2_{total}} = \frac{1}{IIP2_1} + \sum_{i=2}^{n} \frac{G_1 G_2 ... G_{i-1}}{IIP2_i} \quad (8)$$

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + ... + \frac{NF_n - 1}{G_1 G_2 ... G_{n-1}} \quad (9)$$

With regard to the 1dB compression point the value at each stage has been computed using the following format (in linear):

$$P_{1dB\_i} = \frac{1}{\frac{1}{P_{1dB\_i-1} \times G_n} + \frac{1}{P_{1dB\_i}}} \quad (10)$$

where *i* refers to the current component output value and *i-1* to the previous stage output value.
In conclusion, by applying parameters of the off-the-shelf products, the system analysis has produced the results summarized in TABLE 4.

	Obtained values	**Requ.**	**Margin**
Gain before ADC	50 dB	20 dB	30 dB
Total NF	2.36 dB	3 dB	0.64 dB
Total IIP3	-0.02 dBm	-25.42 dBm	25.41 dB
Mixer IIP2	65 dBm	55 dBm	10 dB
Total P1db@ input	-70.5 dBm	-75 dBm	4.5 dB
LNA IIP3	30 dBm	26.6 dBm	3.5 dB

TABLE 4: system analysis results.

III. IMPAIRMENTS COMPENSATION

Nevertheless, the direct-conversion architecture suffers from several RF analog impairments that limit its performance; these are: I/Q imbalance, dc offset, flicker noise and phase noise [6].
Part of this preliminary study aims also at investigating possible mitigation techniques on the digital domain, in order to relax as much as possible the requirements for the analog components.
Here, it is presented a literature review for I/Q imbalance compensation methods that are suitable to our application.

A. I/Q compensation algorithms

In general, three different types of classification for I/Q compensation methods can be found in the literature:

- Data/non data–aided compensation methods: algorithms that exploit or less the knowledge of a block of data in the transmitted packets to achieve their scope [11].
- Time/frequency domain compensation methods: algorithms that process the received signal parameters retrieved by its time domain or frequency domain representation [10].
- Compensation methods for frequency dependent/independent imbalances: algorithms that address I/Q imbalances varying or less with the frequency band of the received signal [12].

In most of the literature, the attention is focused on OFDM systems, as they are particularly affected by such imbalance [13]. Moreover, some of the proposed methods jointly accomplish I/Q mismatch recovery and other relevant parameters estimation, such as DC offset [14][17], channel distortion [15] and frequency offset [16][17].
Typically, in SDR context, solutions that are independent from specific communication standards are privileged. Thus, a preamble (training sequence) independent approach would be preferred.
In addition, as among the required services it is included a spectrum monitoring, FFT operation will be implemented even though no OFDM systems are utilized in the served channels. This entails no preference on the specific signal domain for the algorithm processing.
Finally, because of the wide bandwidth to be processed; the elected compensation method should address frequency-dependent imbalances.
From these preliminary considerations, it ensues that suitable candidates for the proposed application are algorithms like the Interference Cancellation (IC) [18], the Blind Source Separation (BSS) or statistical approaches [11], and compensation methods based on non-linear I/Q imbalance model [19].

IV. CONCLUSIONS

This paper has reported the reasons behind the selection of a direct-conversion architecture and the results of a preliminary system analysis for the receiver linearity requirements. This preliminary study confirms the suitability of such architecture for the proposed application.

Finally, candidate algorithms to improve the effective dynamic range, by reducing the I/Q imbalance, have been presented.

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